

## WHAT IS CLAIMED:

1. A method of manufacturing a semiconductor device, the method comprising:  
forming a transistor having a gate structure over a substrate with a gate dielectric layer therebetween;  
forming an interlayer dielectric over the transistor; and  
forming a silicon-rich silicon oxide layer, having a refractive index (R.I.) greater than 1.6, on an upper surface of the interlayer dielectric.
2. The method according to claim 1, comprising forming the silicon-rich silicon oxide layer with a RI greater than 1.7.
3. The method according to claim 2, comprising forming the silicon-rich silicon oxide layer with a R.I. of 1.7 to 2.0.
4. The method according to claim 2, comprising forming the silicon-rich silicon oxide layer at a thickness of 400 Å to 600 Å.
5. The method according to claim 1, comprising:  
depositing a layer of boron-phosphorous-doped silicate glass (BPSG) as the interlayer dielectric;  
planarizing the upper surface of the BPSG layer; and  
depositing the silicon-rich silicon oxide layer by chemical vapor deposition.
6. The method according to claim 1, comprising depositing the silicon-rich silicon oxide layer by plasma enhanced chemical vapor deposition at a temperature of 450°C to 650°C.
7. The method according to claim 6, comprising depositing the silicon-rich silicon oxide layer at a silane flow rate of 100 to 150 sccm.
8. The method according to claim 7, comprising depositing the silicon-rich silicon oxide layer at:  
an N<sub>2</sub>O flow rate of 165 to 195 sccm;  
an R.F. power of 110 to 140 watts;  
a spacing of 625 to 675 mils; and  
a pressure of 1.8 to 2.2 Torr.
9. The method according to claim 8, comprising depositing the silicon-rich silicon oxide layer for 3 to 15 seconds.
10. The method according to claim 1, wherein the gate structure comprises:  
a tunnel oxide as the gate dielectric layer on the substrate;  
a floating gate electrode on the tunnel oxide;

an interpoly dielectric comprising an oxide/nitride/oxide (ONO) stack on the floating gate; and

a control gate electrode on the interpoly dielectric.

11. The method according to claim 10, comprising:

forming silicon oxide sidewall spacers on the side surfaces of the gate structure;

forming a layer of silicon nitride on an upper surface of the gate stack and on the silicon oxide sidewall spacers; and

thereafter depositing the interlayer dielectric.

12. A semiconductor device comprising:

a transistor having gate structure over a substrate with a gate dielectric layer therebetween; and

a silicon-rich silicon oxide layer, having a refractive index (R.I.) greater than 1.6, on an upper surface of the interlayer dielectric.

13. The semiconductor device according to claim 12, wherein the silicon-rich silicon oxide layer has a R.I. greater than 1.7.

14. The semiconductor device according to claim 13, wherein the silicon-rich silicon oxide layer has a R.I. of 1.7 to 2.0.

15. The semiconductor device according to claim 12, wherein the silicon-rich silicon oxide layer has a thickness of 400°A to 600°A.

16. The semiconductor device according to claim 12, wherein the gate structure comprises:

a tunnel oxide as the gate dielectric layer on the substrate;

a floating gate electrode on the tunnel oxide;

an interpoly dielectric comprising an oxide/nitride/oxide (ONO) stack on the floating gate; and

a control gate electrode on the interpoly dielectric.

17. The semiconductor device according to claim 16, comprising silicon oxide sidewall spacers on side surfaces of the gate structure.

18. The semiconductor device according to claim 17, comprising a layer of silicon nitride on an upper surface of the gate structure and on the silicon oxide sidewall spacers.

19. The semiconductor device according to claim 12, wherein the interlayer dielectric comprises a boron-phosphorous-doped silicate glass (BPSG).